ABSTRACT OF THE DISCLOSURE

In a semiconductor device, source/drain layers have a low resistivity region and an extension region extending from the low resistivity region toward the channel region. The extension regions are lower in impurity concentration and shallower in depth than the low resistivity regions. The device also has a first impurity-doped layer formed in the channel region between the source/drain layers, a second impurity-doped layer formed under the first impurity-doped layer, and a third impurity-doped layer formed under the second impurity-doped layer. The first impurity-doped layer is equal or less in junction depth than the extension regions. The second impurity doped layer has impurity concentration and thickness to be fully depleted due to a built-in potential as created between the first and third impurity-doped layers.